

Title: PIC24FJ256DA210 Dev. Board		
Size: C	03-02183	Rev 1.1
		Eng: P. Tamayo
Date: Mon Apr 26, 2010		Drawn by: S. Humbert
Filename: 03-02183_REV1_1.SCH		Sheet 1 of 3

Use of external SRAM is optional. if internal 24/96 KB RAM cannot Accomodate the required frame buffer for a specific color depth & resolution combination.

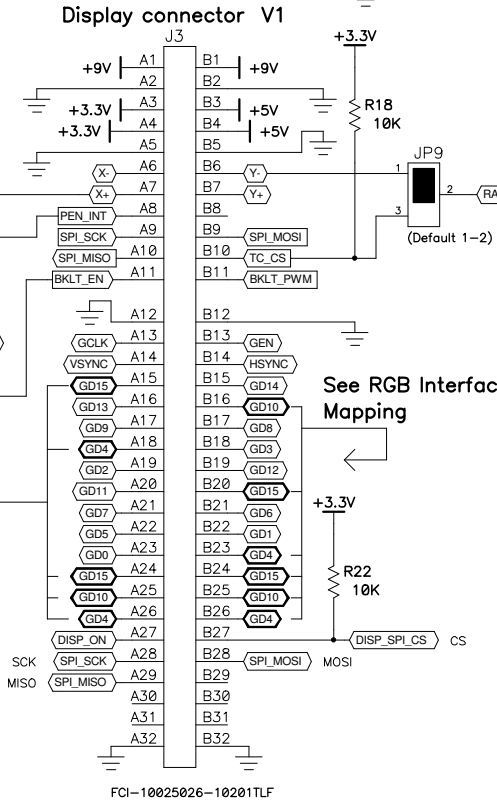
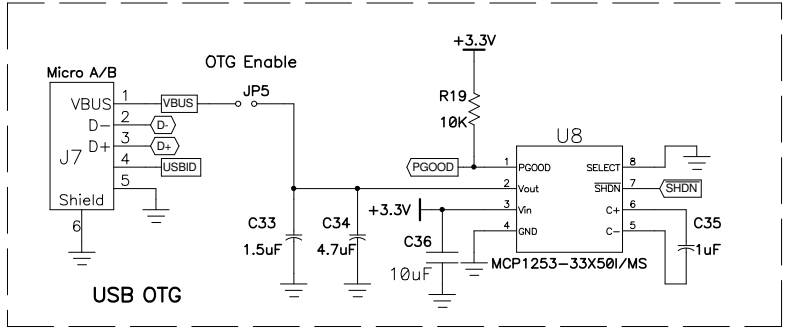
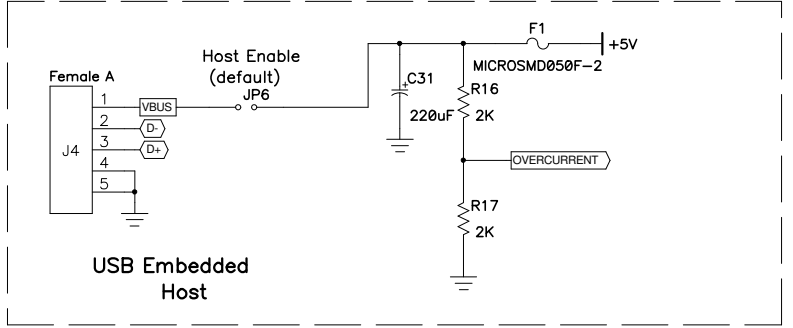
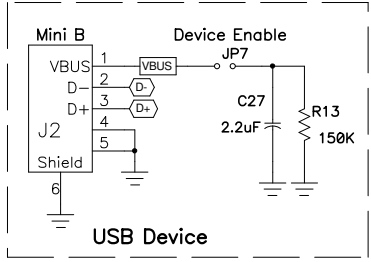
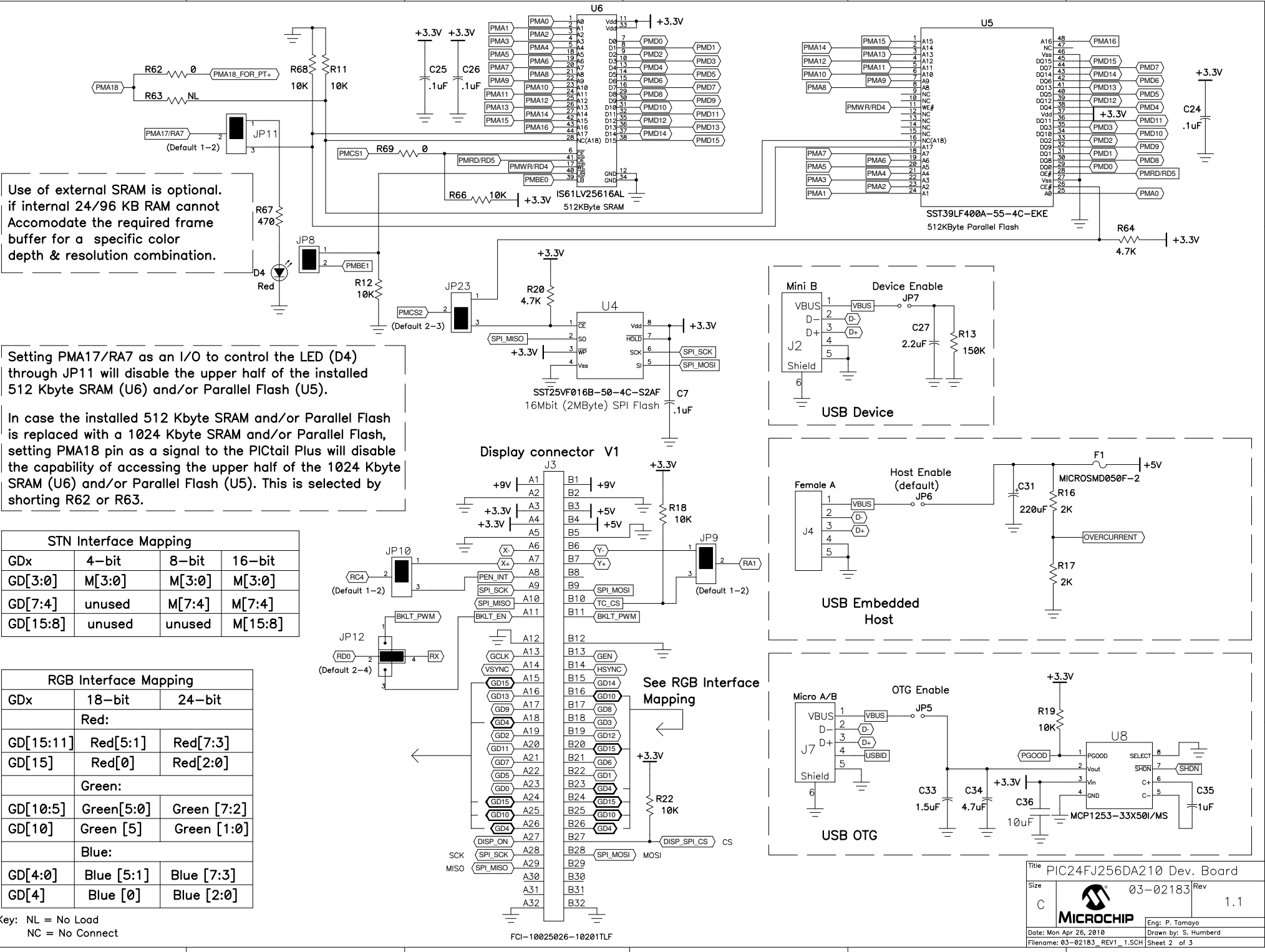
Setting PMA17/RA7 as an I/O to control the LED (D4) through JP11 will disable the upper half of the installed 512 Kbyte SRAM (U6) and/or Parallel Flash (U5).

In case the installed 512 Kbyte SRAM and/or Parallel Flash is replaced with a 1024 Kbyte SRAM and/or Parallel Flash, setting PMA18 pin as a signal to the PICTail Plus will disable the capability of accessing the upper half of the 1024 Kbyte SRAM (U6) and/or Parallel Flash (U5). This is selected by shorting R62 or R63.

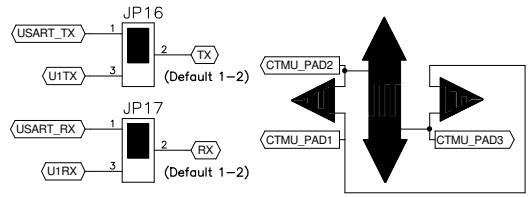
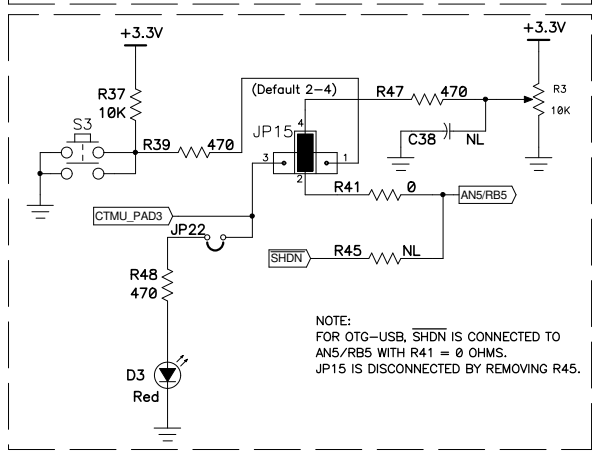
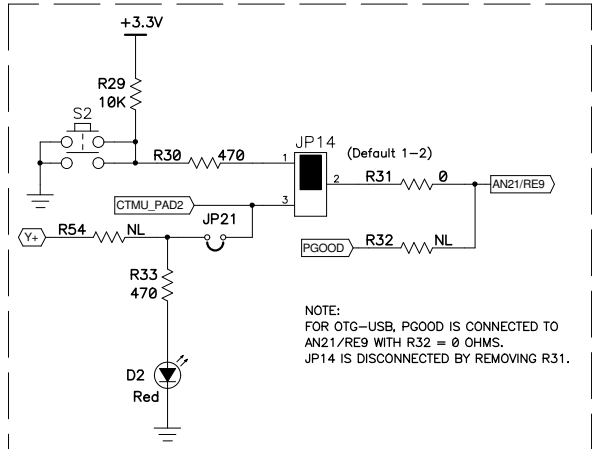
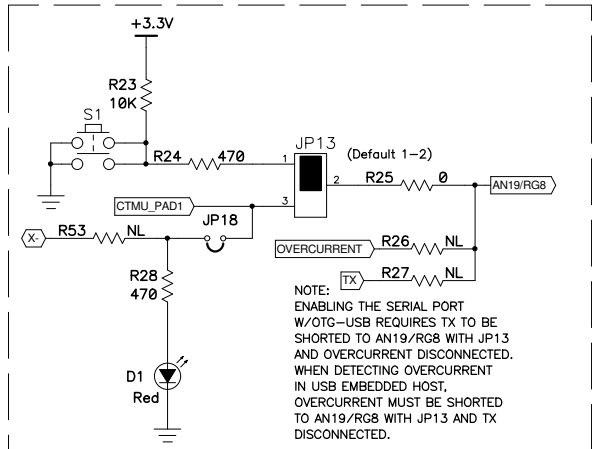
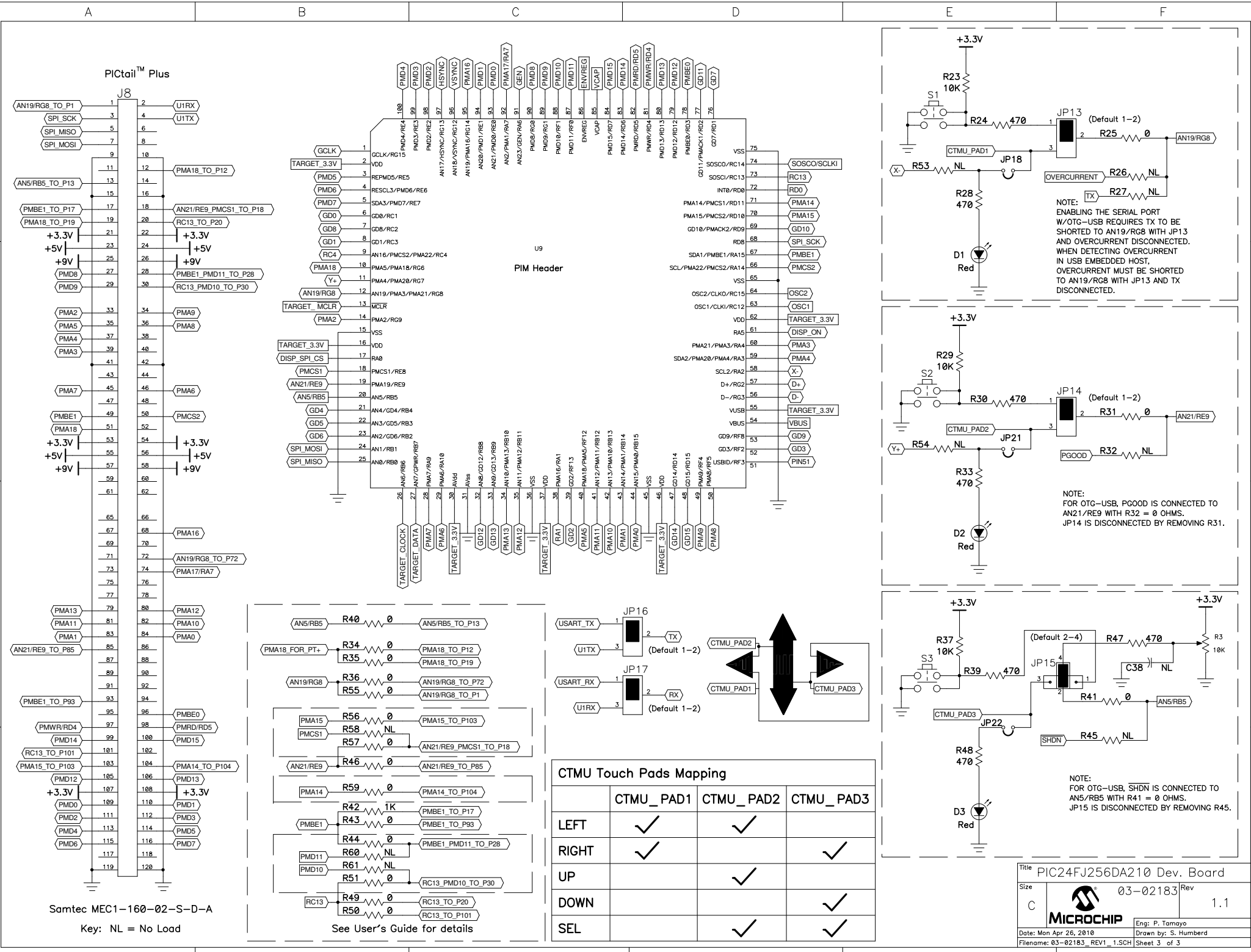
GDx	4-bit	8-bit	16-bit
GD[3:0]	M[3:0]	M[3:0]	M[3:0]
GD[7:4]	unused	M[7:4]	M[7:4]
GD[15:8]	unused	unused	M[15:8]

GDx	18-bit	24-bit
Red:		
GD[15:11]	Red[5:1]	Red[7:3]
GD[15]	Red[0]	Red[2:0]
Green:		
GD[10:5]	Green[5:0]	Green [7:2]
GD[10]	Green [5]	Green [1:0]
Blue:		
GD[4:0]	Blue [5:1]	Blue [7:3]
GD[4]	Blue [0]	Blue [2:0]

Key: NL = No Load
NC = No Connect

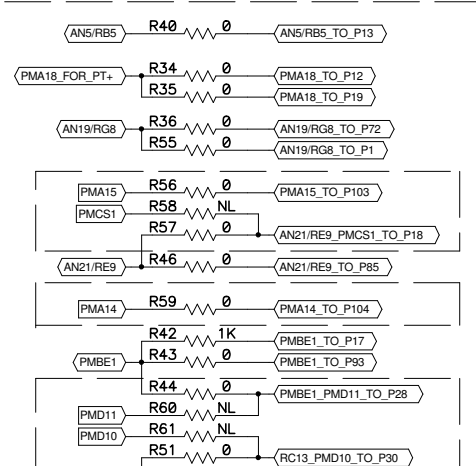
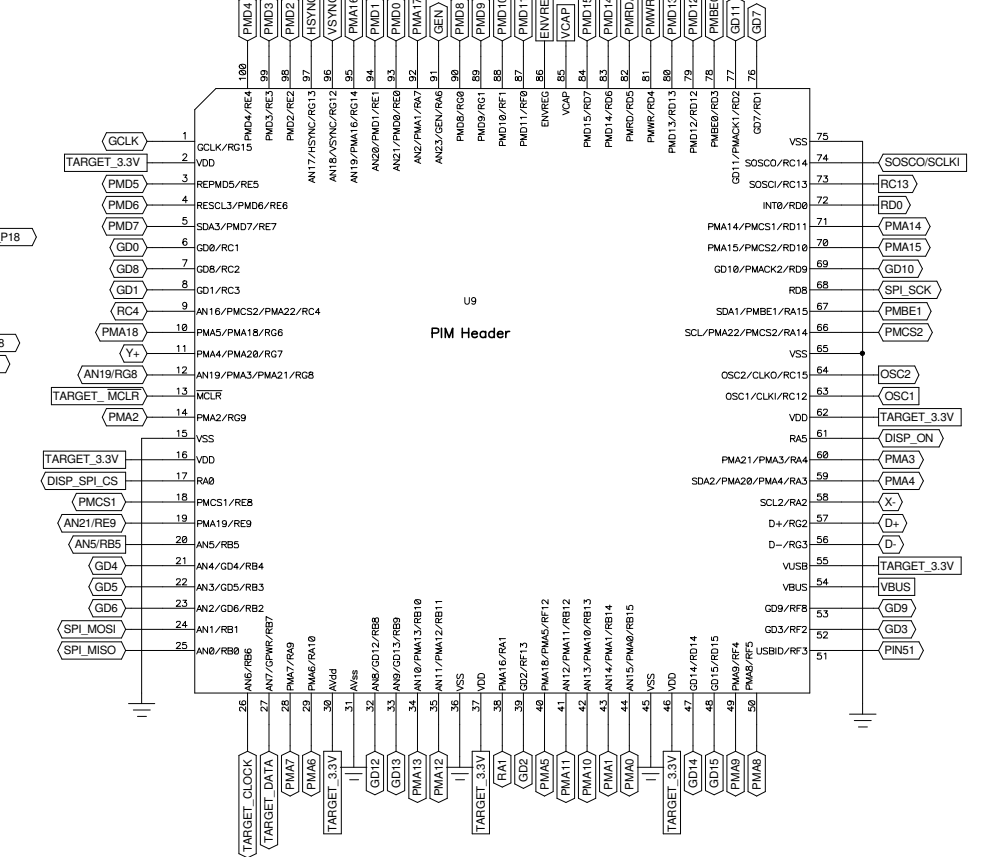
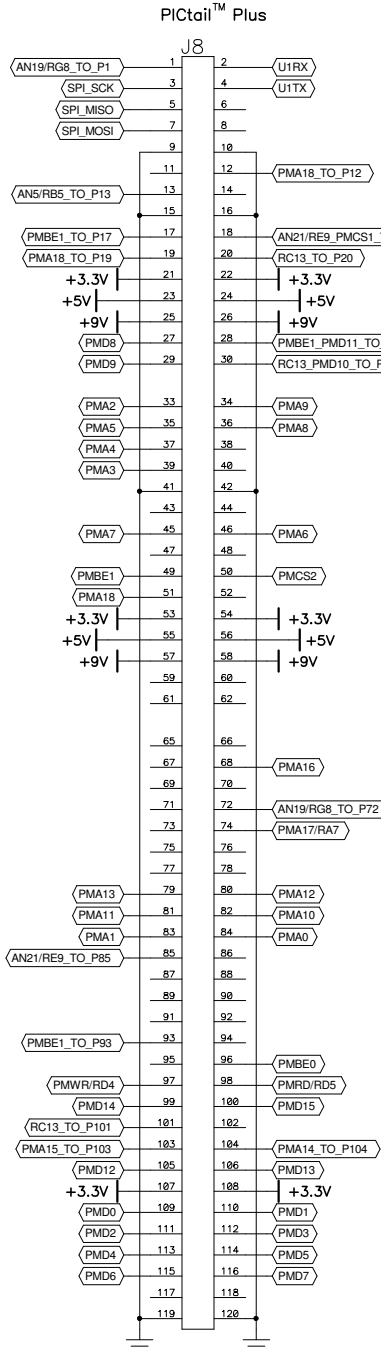


See RGB Interface Mapping



CTMU Touch Pads Mapping

	CTMU_PAD1	CTMU_PAD2	CTMU_PAD3
LEFT	✓	✓	
RIGHT	✓		✓
UP		✓	
DOWN			✓
SEL		✓	✓



Samtec MEC1-160-02-S-D-A
Key: NL = No Load

See User's Guide for details